

2A 650V N-channel Enhancement Mode Power MOSFET

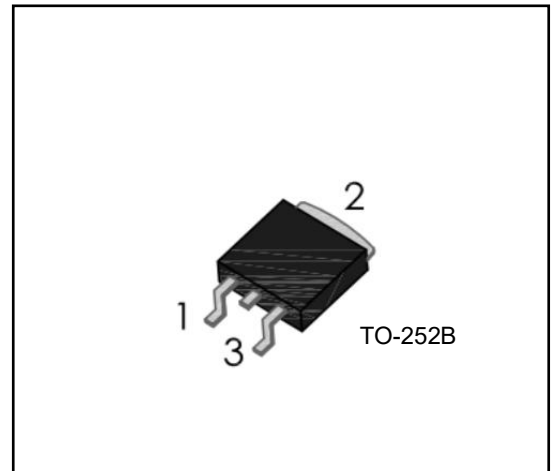
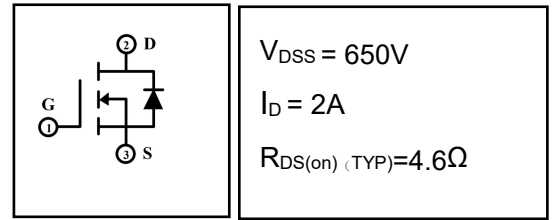
1 Description

These N-channel enhanced vdmofets, is obtained by the self-aligned planar technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. Which accords with the RoHS standard.

- Fast switching
- ESD improved capability
- Low on resistance($R_{dson} \leq 5.5\Omega$)
- Low gate charge(Typ: 9.5nC)
- Low reverse transfer capacitances(Typ: 3pF)
- 100% single pulse avalanche energy test
- 100% ΔV_{DS} test

3 Applications

- Used in various power switching circuit for system miniaturization and higher efficiency.
- Power switch circuit of electron ballast and adaptor.



4 Electrical Characteristics

4.1 Absolute Maximum Ratings (Tc=25°C, unless otherwise noted)

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current(continuous) ^(Note 3)	I_D	2	A
Drain Current(continuous)(T=100°C) ^(Note 3)	I_D	1.3	A
Drain Current(Pulsed)	I_{DM}	8	A
Single Pulse Avalanche Energy ^(Note 4)	E_{AS}	50	mJ
Derating Factor above	$T_a = 25^\circ C$	0.28	W
Power Dissipation	$T_c = 25^\circ C$		
Operating Junction Temperature Range	T_j	-55 ~ 150	°C
Storage Temperature Range	T_{stg}	-55 ~ 150	°C

4.2 Thermal Characteristics

PARAMETER	SYMBOL	VALUE	UNIT
Thermal Resistance, Junction to Case-sink	R_{thJC}	3.57	°C/W
Thermal Resistance, Junction to Ambient	R_{thJA}	100	°C/W

4.3 Electrical Characteristics (Tc=25°C, unless otherwise noted)

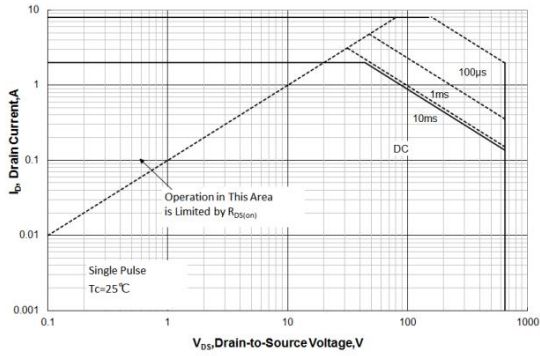
PARAMETER	SYMBOL	Test Condition	VALUE			UNIT
			MIN	TYP	MAX	
Off Characteristics						
Drain-source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	650	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V, T _C =25°C	--	--	1	μA
		V _{DS} =520V, V _{GS} =0V, T _C =125°C	--	--	100	μA
Gate-to-Body Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
On Characteristics (Note 3)						
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	--	4.0	V
Drain-source on Resistance	R _{DS(on)}	V _{GS} =10V, I _D =1.0A	--	4.6	5.5	Ω
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz	--	335	--	pF
Output Capacitance	C _{oss}		--	33	--	
Reverse Transfer Capacitance	C _{rss}		--	3	--	
Turn-on Delay Time	T _{d(on)}	I _D =2A, V _{DD} =325V, V _{GS} =10V, R _G =10Ω	--	11	--	ns
Turn-on Rise Time	t _r		--	13	--	
Turn-off Delay Time	T _{d(off)}		--	29	--	
Turn-off Fall	t _f		--	12	--	
Total Gate Charge	Q _g	I _D =2A, V _{DD} =520V, V _{GS} =10V	--	9.5	--	nC
Gate-to-Source Charge	Q _{gs}		--	1.5	--	
Gate-to-Drain("Miller")C harge	Q _{gd}		--	4.9	--	
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{FSD}	V _{GS} =0V, I _S =2A	--	--	1.5	V
Continuous Source Current (BodyDiode) (Note 3)	I _S		--	--	2	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =2A, dI _F /dt=100A/μS, V _{GS} =0V	--	187	--	ns
Reverse Recovery Charge	Q _{rr}		--	610	--	nC

Notes:

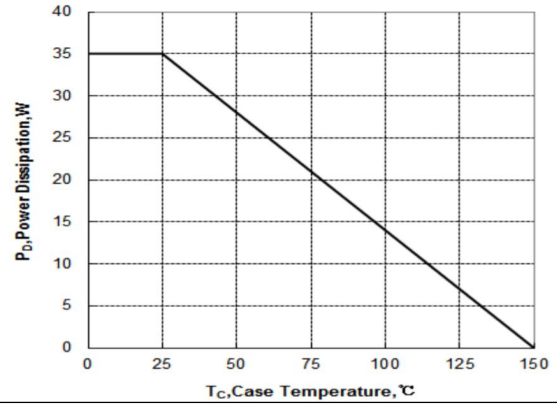
- 1: Repetitive rating, pulse width limited by maximum junction temperature.
- 2: Surface mounted on FR4 Board, t≤10sec.
- 3: Pulse width ≤ 300μs, duty cycle ≤ 2%.
- 4: L=10mH, I_D=3.1A, V_{DD}=50V, Start T_J=25°C.

5 Typical Test Circuit and Waveform

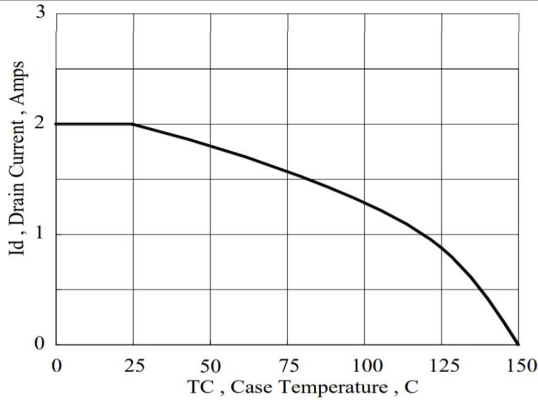
<p style="text-align: center;">Gate Charge Test Circuit</p>	<p style="text-align: center;">Gate Charge Waveforms</p>
<p style="text-align: center;">Resistive Switching Test Circuit</p>	<p style="text-align: center;">Resistive Switching Waveforms</p>
<p style="text-align: center;">Diode Reverse Recovery Test Circuit</p>	<p style="text-align: center;">Diode Reverse Recovery Waveform</p> $E_{AS} = \frac{I_{AS}^2 L}{2}$
<p style="text-align: center;">Unclamped Inductive Switching Test Circuit</p>	<p style="text-align: center;">Unclamped Inductive Switching Waveform</p>



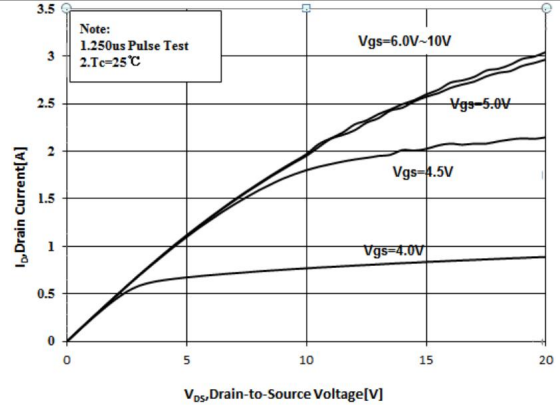
Maximum Forward Bias Safe Operating Area



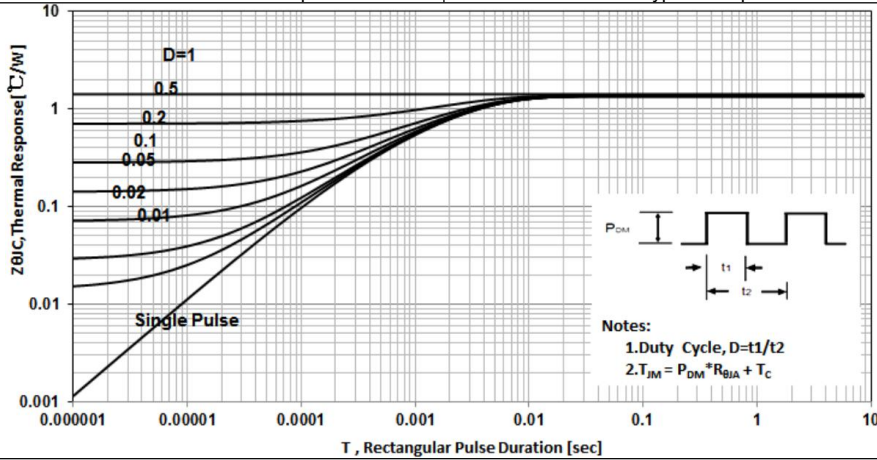
Maximum Power Dissipation vs Case Temperature



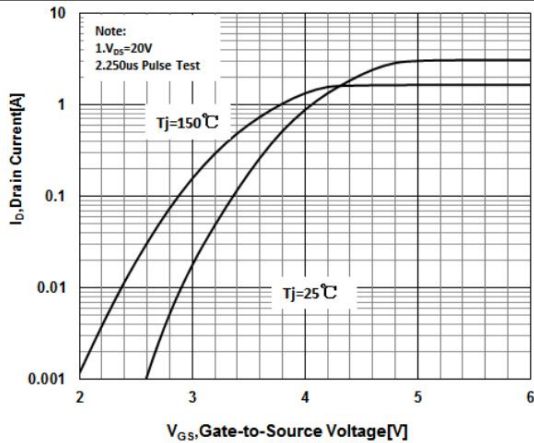
Maximum Continuous Drain Current vs Case Temperature



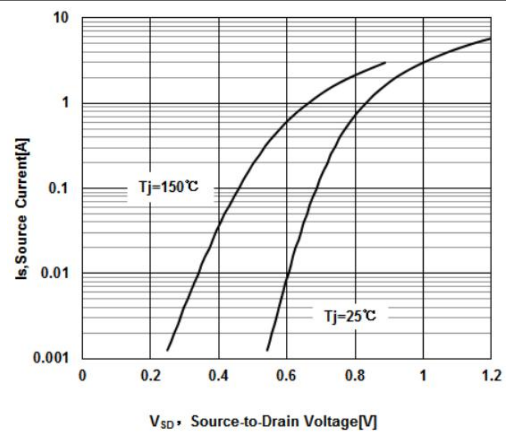
Typical Output Characteristics



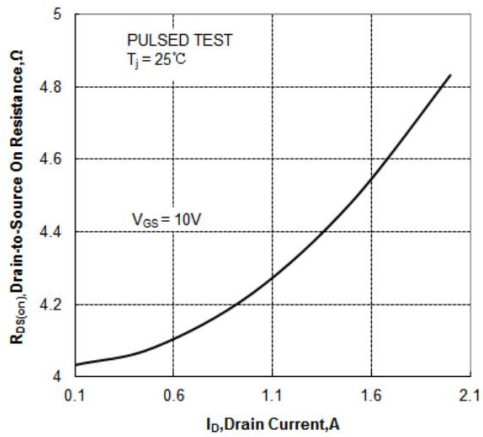
Maximum Effective Thermal Impedance, Junction to Case



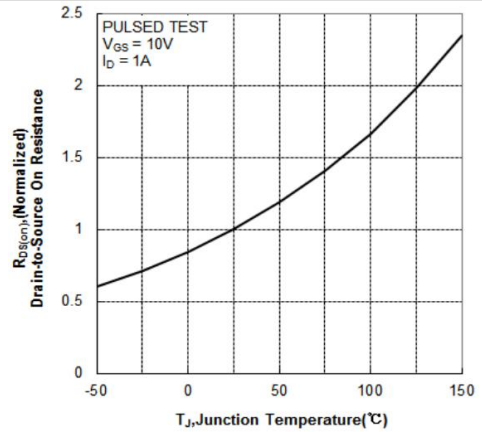
Typical Transfer Characteristics



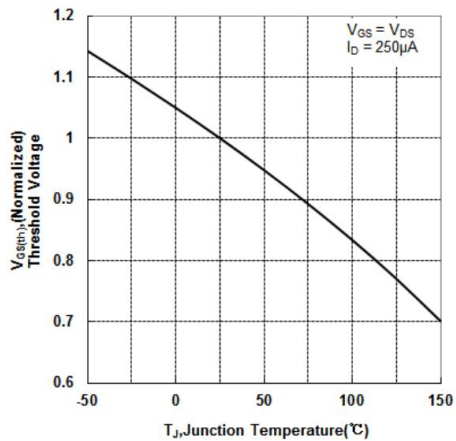
Typical Body Diode Transfer Characteristics



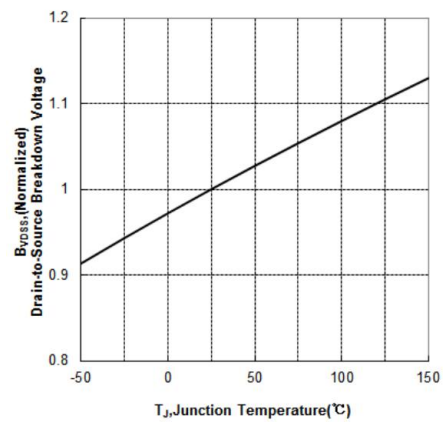
Typical Drain to Source ON Resistance vs Drain Current



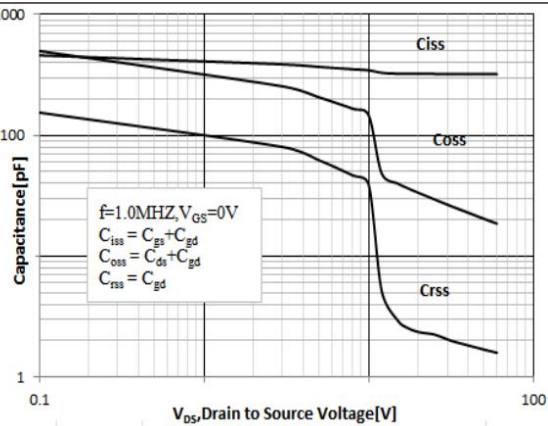
Typical Drain to Source on Resistance vs Junction Temperature



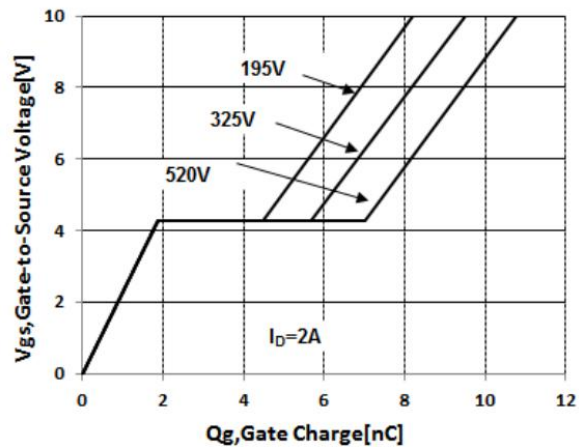
Typical Threshold Voltage vs Junction Temperature



Typical Breakdown Voltage vs Junction Temperature



Typical Capacitance vs Drain to Source Voltage



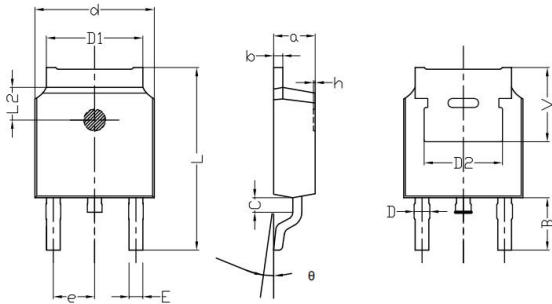
Typical Gate Charge vs Gate to Source Voltage

8 Product Specifications and Packaging Models

Product Model	Package Type	Mark Name	RoHS	Package	Quantity
D2N65	TO-252	D2N65	Pb-free	Braid	2500/disc

9 Dimensions

TO-252 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	min.	max.	min.	max.
a	2.20	2.40	0.087	0.095
b	0.46	0.58	0.018	0.023
c	0.70	0.90	0.028	0.035
D	0.80	0.90	0.032	0.035
d	6.50	6.70	0.2561	0.2640
D1	5.10	5.46	0.201	0.215
D2	4.73	4.93	0.1864	0.1942
A	6.00	6.20	0.2364	0.2443
e	2.19	2.39	0.0861	0.0940
L	10.40	11.00	0.4098	0.4334
B	3.5	3.7	0.1379	0.1458
L2	1.5	1.7	0.0591	0.0670
θ	0	8	0	8
h	0	0.3	0	0.0118
V	5.25	5.45	0.2069	0.2147
E	0.6	0.8	0.0236	0.0315

10 Attentions

- Jianguo Donghai Semiconductor Technology Co., Ltd. reserves the right to change the specification without prior notice! The customer should obtain the latest version of the information before making the order and verify that the information is complete and up to date.
- It is the responsibility of the purchaser for any failure or failure of any semiconductor product under certain conditions. It is the responsibility of the purchaser to comply with safety standards and to take safety measures in the system design and machine manufacturing of WXDH products in order to avoid potential risk of failure. Injury or property damage.
- Product promotion is endless, our company will be dedicated to provide customers with better products.

11 Appendix

Revision history:

Date	REV.	Description	Page
2020.03.09	1.0	Original	